

### REMARKS

Filed concurrently herewith is a Request for a One-Month Extension of Time which extends the shortened statutory period for response to July 1, 2006. Accordingly, Applicant respectfully submits that this response is being timely filed under the next business day rule.

The Official Action dated May 1, 2006 has been received and its contents noted. The Examiner is thanked for his consideration of this application.

Claims 1-3 and 21-32 are pending for consideration, of which claims 1 and 21 are independent. Claims 4-20 have been canceled previously as being directed to non-elected species.

In the detailed Office Action, claims 1-3, 21, 22 and 25-28 stand rejected under 35 U.S.C. §102(b) as anticipated by Altmann (U.S. Patent No. 6,448,848 – previously cited). Further, claim 30 stands rejected under 35 U.S.C. §103(a) as unpatentable over Altmann. Finally, claims 23, 24, 29, 31 and 32 stand objected to as being dependent upon a rejected base claim. These rejections and objection are respectfully traversed at least for the reasons provided below.

In the Office Action, the Examiner equates Applicant's common node (i.e., node N in Applicant's Fig. 1) to the common sources of NMOS FETs  $M_1$  and  $M_2$  in  $g_m$  cell 110 in Altmann's Fig. 1. The Examiner further equates Applicant's recited current source to one or both of the PMOS FETs 115 of Altmann, and Applicant's recited comparison circuit to the combination of  $g_m$  cell 120 and amplifier A(s) of Altmann. In response, Applicant's will show below that Altmann's circuits, when analyzed according to Altmann's teaching and to proper understanding circuit theory, do not correspond to Applicant's claimed features and, therefore, do not perform the same functions as Applicant's claimed invention.

In order to facilitate the comparison of Applicant's claimed invention with that of Altmann, Applicant attaches herewith a marked-up Fig. 1 of Altmann and two pages of publication directed to Thevenin's, Norton's, and Maximum Power Transfer Theorems, specifically to ideal current sources.

Referring to Altmann's Fig. 1, Applicant notes current  $I_1$  flowing from a supply line at the top of the drawing to a current source line at the bottom of the drawing. This bottom line is identified indirectly as the current source line in Col. 2, lines 42-46 of Altmann because it is the line to which capacitors  $C_1$  and  $C_2$  are tied. The current source line is

connected to ground, as denoted by the ground symbol in Fig. 1. Since  $M_1$  and  $M_2$  are NMOS transistors (see Col. 2, lines 27-28 of Altmann), their common sources must be the on the ground side, and the common node must therefore be the point at which  $M_1$  and  $M_2$  are connected to the circuit element indicated by two intersecting circles, which is connected to the source line. This pair of intersecting circles, although not explicitly identified by Altmann, would be understood by a person skilled in the art to indicate a current source, a circuit that (ideally) outputs a constant current regardless of the load imposed on it.

At this point, Applicant would like to point the Examiner's attention to the attached publication regarding Thevenin's, Norton's, and Maximum Power Transfer Theorems which defines "ideal current source" and shows the symbol representing ideal current source as two intersecting circles; and, incidentally, Applicant notes that this circuit element (i.e., the current source denoted by the two intersecting circles) of Altmann is most closely identified with Applicant's current source recited in claim 1, and that the Examiner's assertion that either or both of FETs 115 is equivalent to Applicant's claimed current source is insupportable.

As summarized above, in the rejection, the Examiner asserts that the PMOS transistor 115 are equivalent to Applicant's claimed current source. However, Applicant respectfully asserts that the PMOS transistors 115 of Altmann cannot be identified as an equivalence of Applicant's claimed current source because the PMOS transistors 115 are connected to the drains, not the sources, of the NMOS transistors  $M_1$  and  $M_2$ , and therefore are not connected to the "common node" as alleged by the Examiner.

Moreover, Applicant respectfully assert that one skilled in the art would also recognize the pair of PMOS transistors 115 in Altmann's Fig. 1 as load elements, not a current source, that conduct varying currents ( $I_1/2 + I_3$  and  $I_1/2 + I_4$ , or  $I_1 + I_3 + I_4$  in total) that depend in part on the control signal supplied by amplifier A(s) to transistors  $M_3$  and  $M_4$ .

With respect to the comparison circuit recited in claim 1, Applicants respectfully assert that the claimed comparison circuit receives the same bias signal as the current source and mirrors the current supplied by the current source to the common node. However, in Altmann's Fig. 1, although it appears that the PMOS transistors in  $g_m$  cell 120 receive the same bias signal as the PMOS transistors 115 in  $g_m$  cell 110, this does not imply that the PMOS transistors mirror any of the currents ( $I_1/2 + I_3$ ,  $I_1/2 + I_4$ , or  $I_1 + I_3 + I_4$ ) conducted by the PMOS transistors 115 singly or in combination. The reason is that while the PMOS

transistors 115 in  $g_m$  cell 110 carry both a constant current  $I_1$  flowing toward the bottom of the cell and variable currents ( $I_3$  and  $I_4$ ) flowing out from the cell, the PMOS transistors in  $g_m$  cell 120 carry only the constant current  $I_1$ . Accordingly,  $g_m$  cell 120 and amplifier A(s) do not correspond to Applicant's comparison circuit recited in claim 1.

The Examiner's assertion that the NMOS transistors  $M_1$  and  $M_2$  in Altmann's Fig. 1 are equivalent to Applicant's switches is also improper. When Fig. 1 is interpreted in relation to the discussion in Col. 1, lines 13-32 of Altmann, it becomes clear to the skilled artisan that transistors  $M_1$  and  $M_2$  function as amplifying elements rather than switching elements.

With respect to the anticipatory rejection of independent claim 21 and its respective dependent claim, the arguments set forth above in relation to the rejection of claim 1 are also applicable. In comparison of Applicant's claim 1 and claim 21, the common node of claim 1 is recited as a first node in claim 21, the current source is recited as a first transistor, and its bias signal is recited as the voltage at a second node. In addition to the arguments set forth above, Applicant would like to add the following remarks with respect to claim 21.

The comparison circuit recited in claim 21 compares a current generated from the second node voltage with a reference current. On the other hand, in Altmann's  $g_m$  cell 120, the constant current  $I_1$  output by the current source denoted by intersecting circles is forced through a varying resistance (i.e., the resistance offered by the NMOS transistors varies according to the signals out and outb supplied to their gate electrodes) and the resulting variable voltage is compared with a reference voltage (i.e., CM ref). Although Altmann does not specifically state that 'CM ref' is a voltage, the use of the terms 'CM voltage' and 'CM reference' in claims 1 and 2 of Altmann implies that CM ref in Fig. 1 is a voltage. Accordingly, while Applicant's comparison circuit recited in claim 21 compares a variable current with a reference current, Altmann's  $g_m$  cell 120 and amplifier A(s) compare a variable voltage generated from a constant current and variable resistance with a reference voltage. Hence, the comparison circuit of the presently claimed invention differs from Altmann's  $g_m$  cell 120 and amplifier A(s).

Further, as submitted in the Amendment filed January 9, 2006, the present invention is a feed-forward circuit while Altmann's is a feedback circuit, as disclosed in Col. 2, lines 50-52, claims 1-3, claims 5-7, etc. All of the arguments previously submitted are incorporate herein by reference.

Consequently, since each and every feature of the present claims is not taught (and is

not inherent) in the teachings of Altmann, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1-3, 21, 22 and 25-28, under 35 U.S.C. §102(b), as anticipated by Altmann is improper.

With respect to the obviousness rejection of claim 30, the arguments set forth above in relation to the rejection of independent claims 1 and 21 are also applicable.

In view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-3 and 21-32 be allowed and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,



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